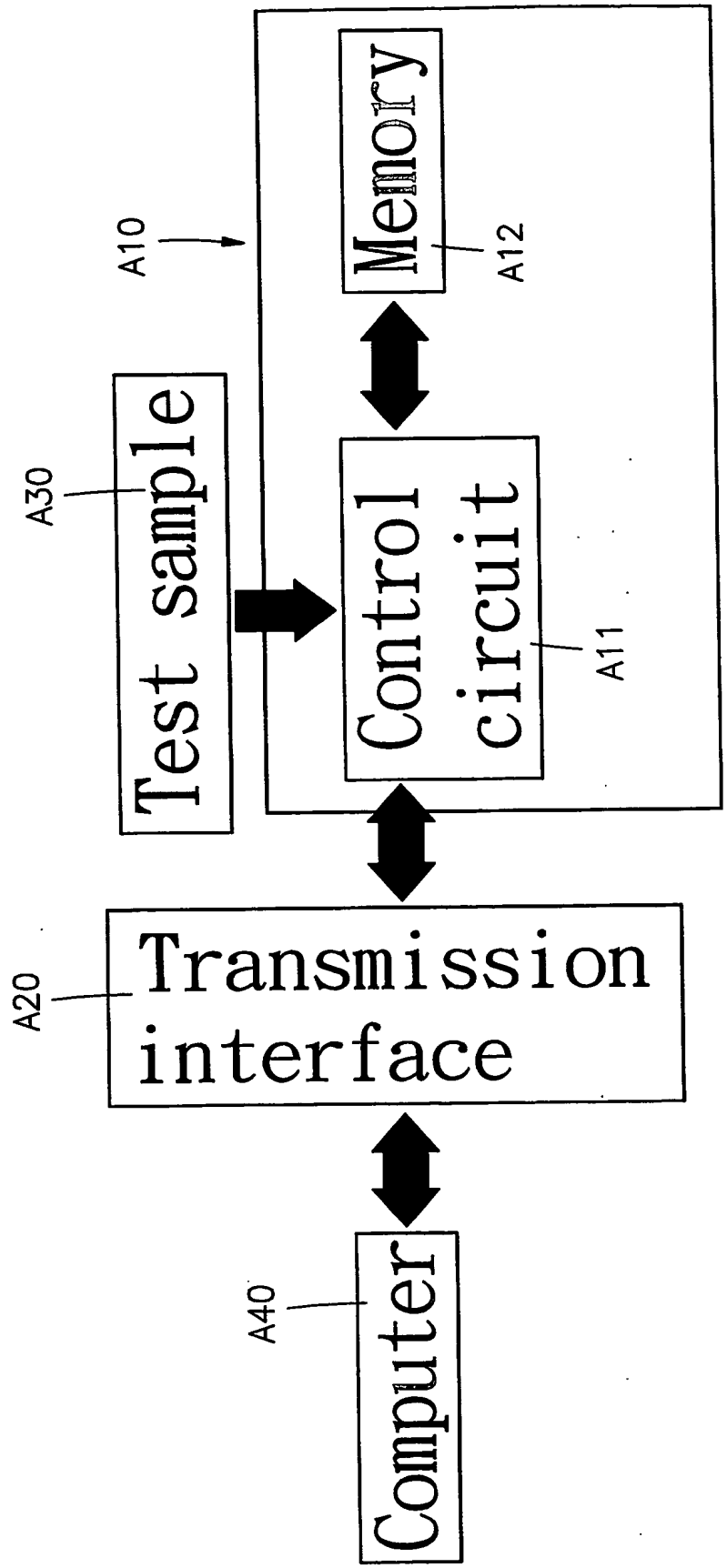
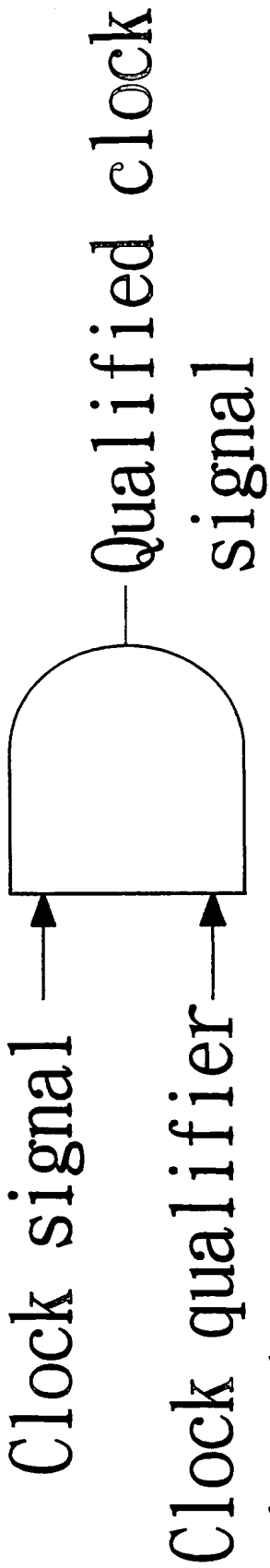
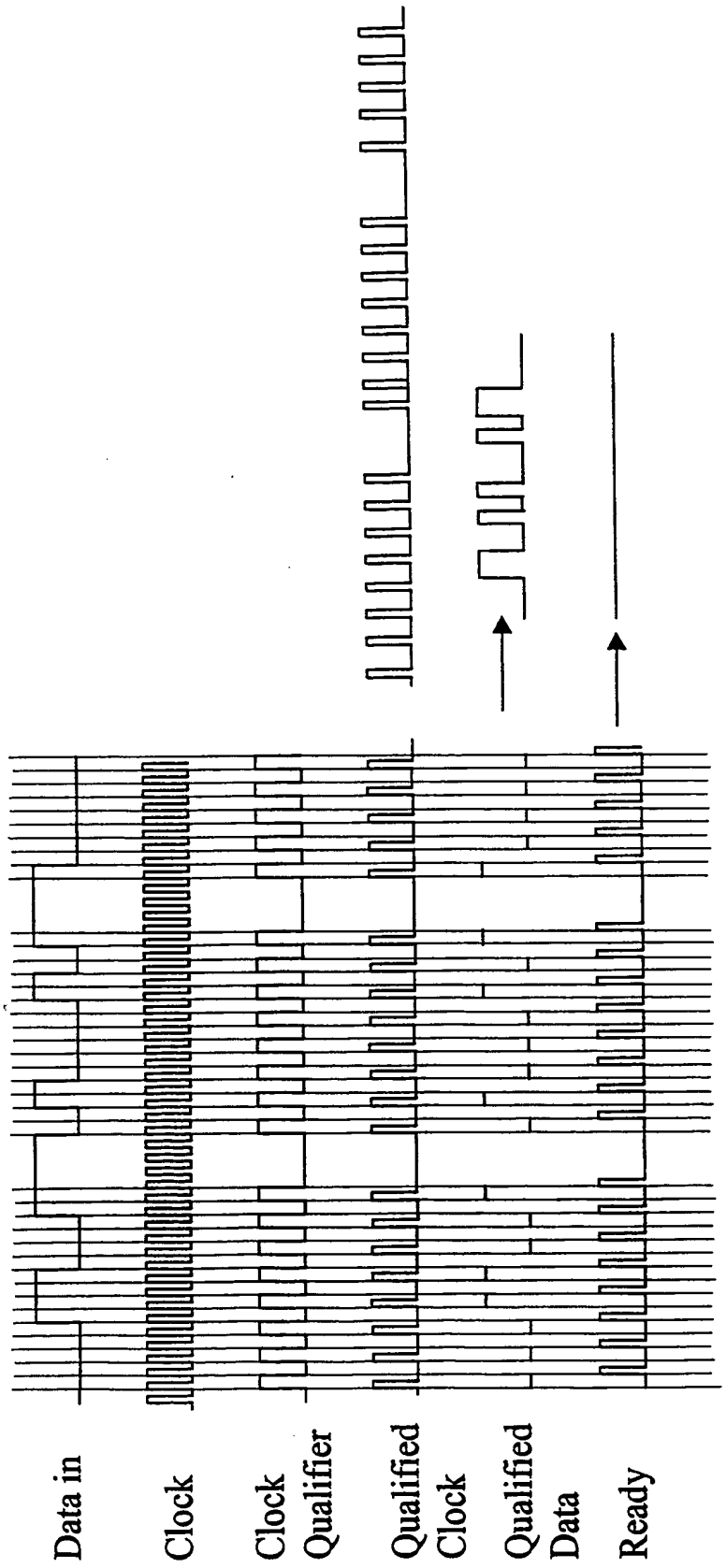


PRIOR ART
FIG. 1



PRIOR ART
FIG.2



PRIOR ART

FIG.3

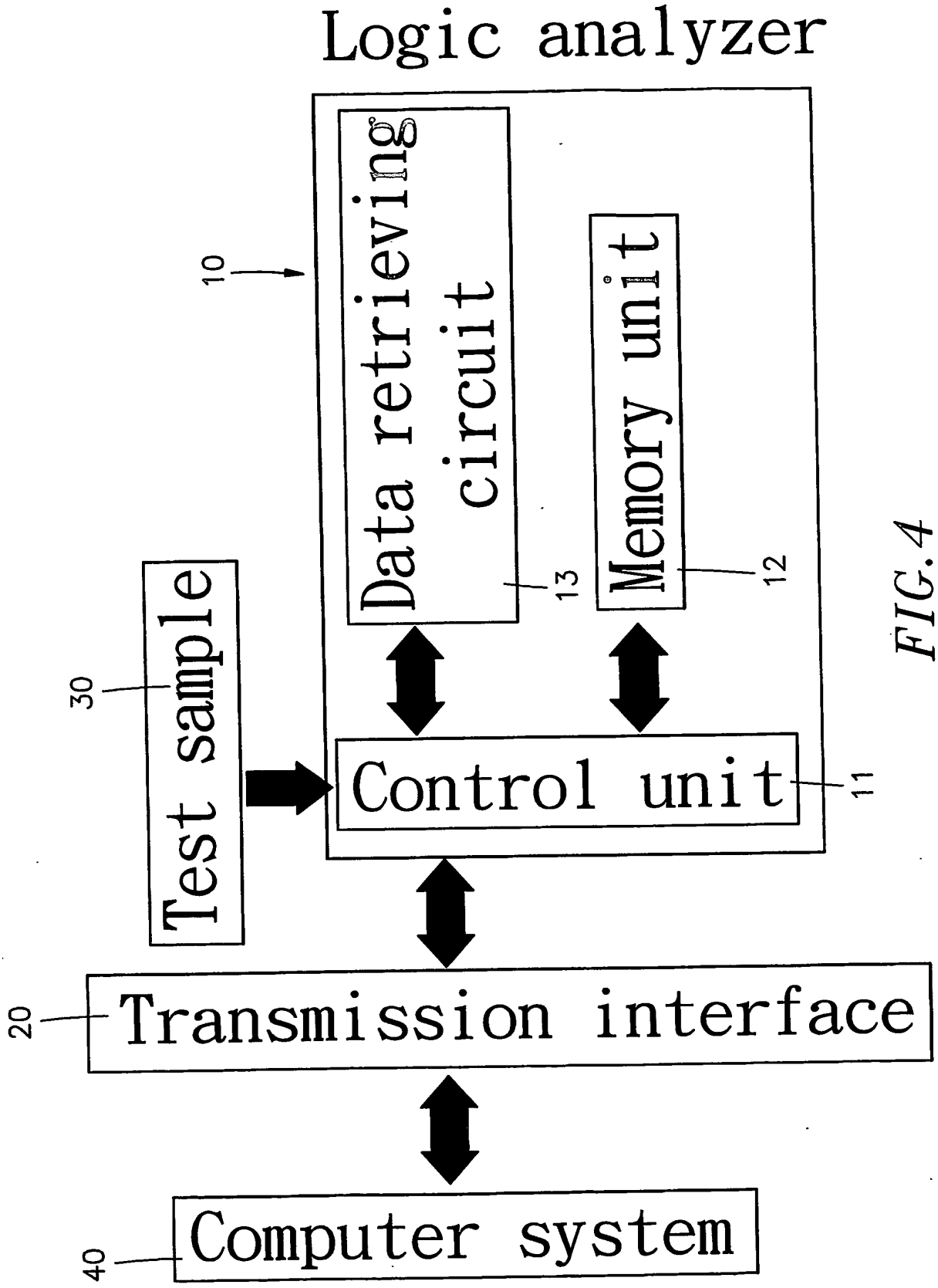

Logic analyzer
10
Data retrieving circuit
13
Memory unit
12
Test sample
30
Control unit
11
Transmission interface
20
Computer system
40

FIG.4

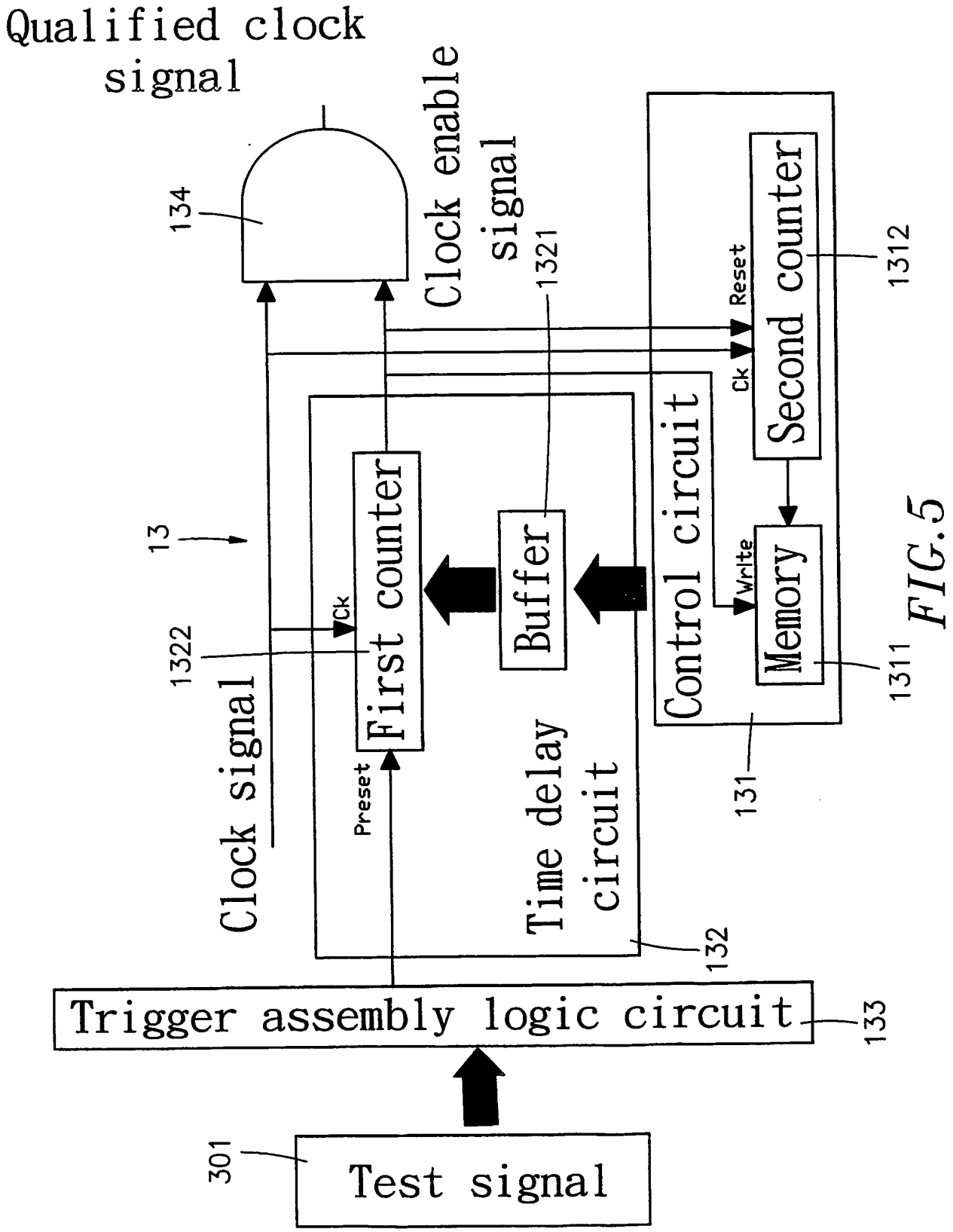

Qualified clock signal
134
Clock enable signal
1321
Reset
Second counter
1312
Ck
Control circuit
13
Ck
First counter
Buffer
Write
Memory
1311
1322
Clock signal
Preset
Time delay circuit
131
132
Trigger assembly logic circuit
133
301
Test signal

FIG.5

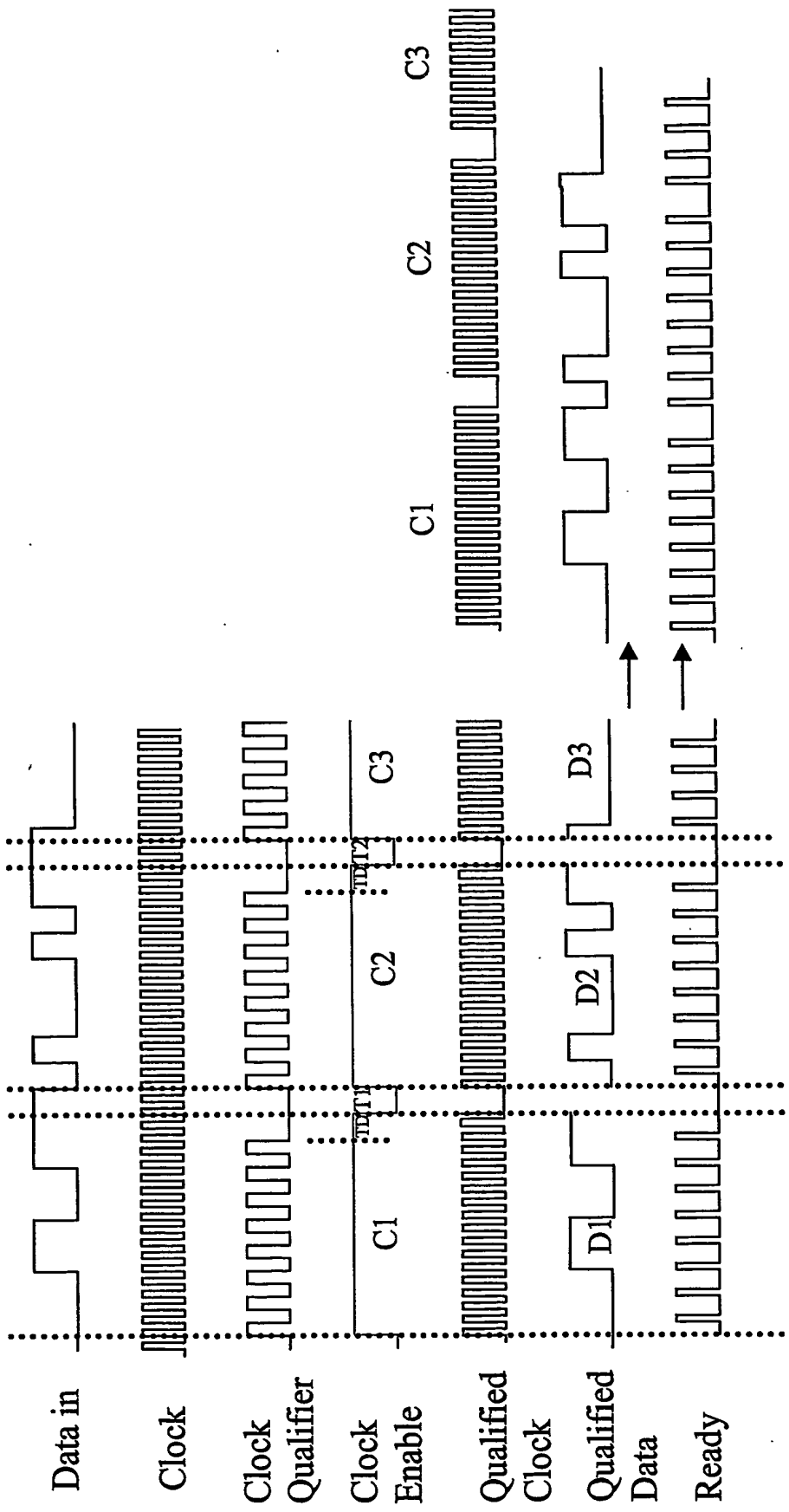

Data in
Clock
Clock Qualifier
Clock Enable
Qualified Clock
Qualified Data
Ready
C1
C2
C3
D1
D2
D3
tDT1
tDT2

FIG.6

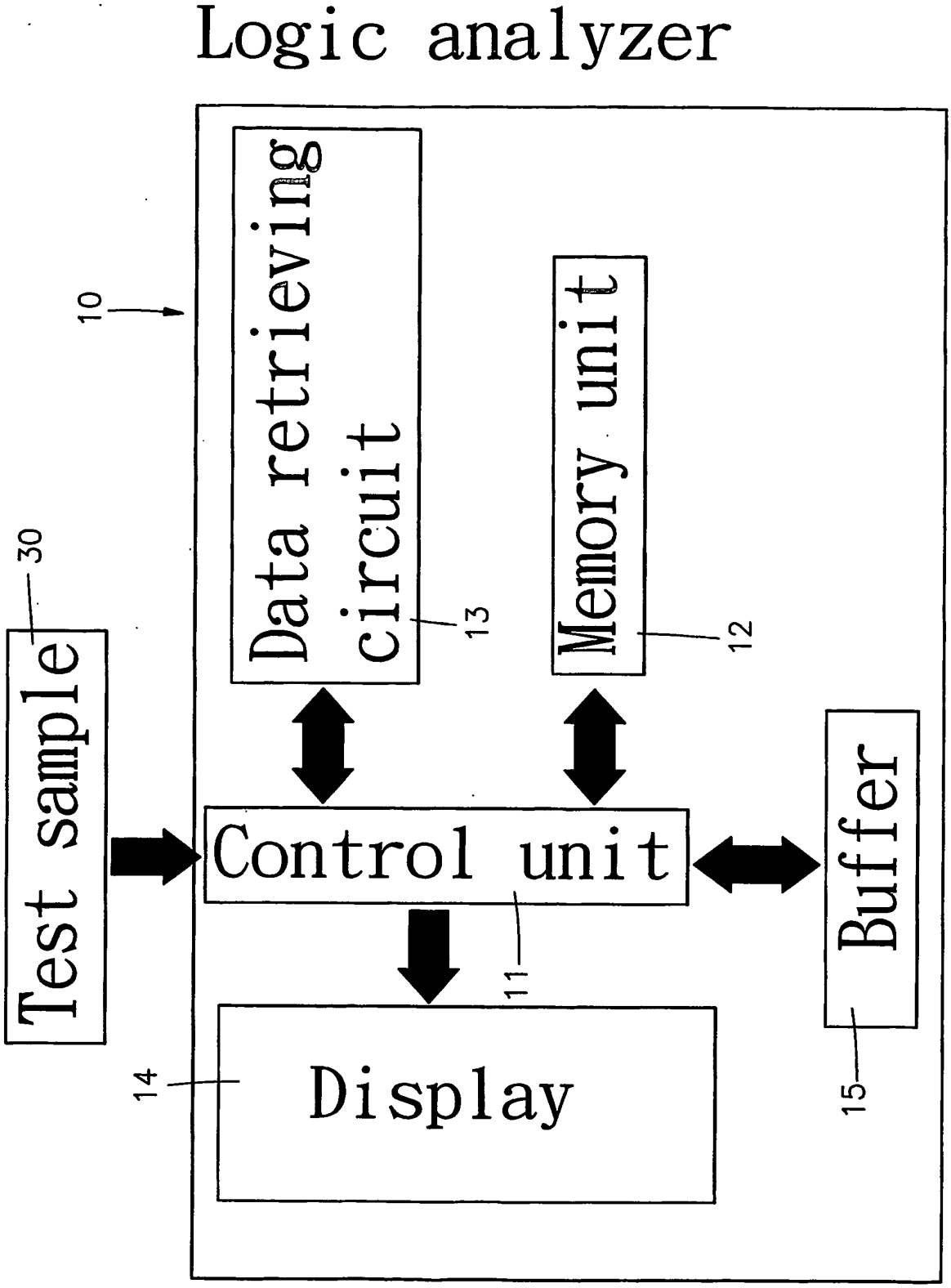

Logic analyzer
10
Data retrieving circuit
13
Memory unit
12
30
Test sample
Control unit
11
Buffer
15
14
Display

FIG. 7